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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 05/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/607,815	BATCHER, KENNETH W.	
	Examiner	Art Unit	
	Tonia L. Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 14 and 20 are objected to because of the following informalities:

a. In claim 14, line 1, please insert the limitation "the", after the limitation "wherein",

b. In claim 20, line 2, please change the limitation "generate" to "generates".

2. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Shridhar et al., U.S. Patent Number 5,727,194 (herein referred to as Shridhar).

5. Referring to claims 1 and 8, Shridhar has taught a method of operating a processor to repeatedly execute an instruction;

a. loading a register with a count value indicative of the number of times the single instruction is to be executed (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 146);

b. fetching and executing a REPEAT instruction, the REPEAT instruction indicating the single instruction to be repeatedly re-executed (Shridhar, column 2 line 20-column 4,

line 12, figures 1 and 2, column 3, lines 5-8, The instructions that load values into elements 140 and 142 indicate the associated instruction(s) to be repeatedly executed.);

c. fetching the single instruction (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 112); and

d. repeatedly executing the single instruction for a consecutive number of times as indicated by the count value (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 146) without refetching the associated instruction (Shridhar column 2 lines 20-23 and 31-45).

2. Referring to claim 2, Shridhar has taught a method of operating a processor to repeatedly execute a single instruction and to repeatedly execute a block of instructions,

a. fetching a REPEAT instruction (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 112, column 3, lines 5-8, The instructions that load values into elements 140, 142, and 146.);

b. executing a REPEAT instruction, wherein execution of the REPEAT instruction stores in a register a count value indicative of the number of times a single instruction is to be executed (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, column 3, lines 5-8, The instructions that load values into elements 140, 142, and 146 indicate the number of times instruction(s) are to be repeatedly executed.);

c. fetching the single instruction (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 112); and

d. repeatedly executing the single instruction consecutively for as many times as indicated by the count value (Shridhar, column 2 line 20-column 4, line 12, figures 1 and

2) without re-fetching the single instruction and without fetching any other instruction (Shridhar column 2 lines 20-23 and 31-45);

e. decrementing the count value in the register each time the single instruction is executed (Shridhar, column 2 lines 20-23 and 31-45);

f. incrementing a program counter once the count value in the register is one of less than zero and equal to zero, thereby providing an effective data rate of one transfer every clock cycle (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 148).

2. Referring to claim 3, Shridhar has taught a method of operating a processor to repeatedly execute a single instruction and to repeatedly execute a block of instructions (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2),

a. loading a register with a count value indicative of the number of times a single instruction is to be executed (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 146);

b. fetching and executing a REPEAT instruction indicating the single instruction that is to be repeatedly executed (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, column 3, lines 5-8, The instructions that load values into elements 140 and 142 indicate the instruction(s) to be repeatedly executed.);

c. incrementing a program counter (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 148);

d. fetching the single instruction (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 112); and

e. repeatedly executing the single instruction for as many times as indicated by a count value stored in the count register (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 146) without re-fetching the single instruction and without fetching any other instruction (Shridhar, column 2 lines 20-23 and 31-45);

f. decrementing the count value in the register each time the single instruction is executed (Shridhar, figures 1 and 2, column 2 lines 20-23 and 31-45, element 150);

g. stalling the program counter once the count value in the register is one of less than zero and equal to zero, thereby providing an effective data rate of one transfer every clock cycle (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2).

2. Referring to claim 4, Shridhar has taught the method of operating a processor according to claim 3, as described above, wherein said count value is stored in said count register before execution of said REPEAT instruction (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 146).

3. Referring to claim 5, Shridhar has taught the method of operating a processor according to claim 3, as described above, wherein said REPEAT instruction includes the count value that is stored in said count register, wherein execution of the REPEAT instruction stores the count value in said count register (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 146).

4. Referring to claim 6, Shridhar has taught the method of operating a processor according to claim 3, as described above, wherein said method further comprises: incrementing the program counter after the associated instruction has been executed for as many times as indicated by the count value (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 148).

5. Referring to claim 7, Shridhar has taught the method according to claim 3, as described above, wherein method further comprises: decrementing said count value stored in said register each time said associated instruction is executed; and determining whether said count value is less than or equal to zero (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 154).

6. Referring to claim 9, Shridhar has taught a processor for repeatedly executing a single instruction and to repeatedly execute a block of instructions,

a. fetch means for fetching a REPEAT instruction (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 112, column 3, lines 5-8, The instructions that load values into elements 140, 142, and 146.);

b. execute means for executing a REPEAT instruction, wherein execution of the REPEAT instruction stores in a register a count value indicative of the number of times the instruction is to be executed (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, column 3, lines 5-8, element 116, The instructions that load values into elements 140, 142, and 146 indicate the number of times instruction(s) are to be repeatedly executed.);

c. fetch means for fetching the associated instruction (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 112); and

d. execute means for executing the associated instruction for as many times as indicated by the count value (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 146) without re-fetching the single instruction and without fetching any other instruction (Shridhar, column 2 lines 20-23 and 31-45);

e. means for decrementing the count value in the register each time the single instruction is executed (Shridhar, column 2 lines 20-23 and 31-45, Figures 1 and 2, element 150);

f. means for incrementing a program counter once the count value in the register is one of less than zero and equal to zero, thereby providing an effective data rate of one transfer every clock cycle (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 148).

2. Referring to claim 10, Shridhar has taught a processor for repeatedly executing a single instruction and to repeatedly execute a block of instructions (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2),

a. load means for loading a register with a count value indicative of the number of times a single instruction is to be executed (Shridhar, column 2 lines 20-23 and 31-45, figures 1 and 2, elements 100, 150, 151, and 146);

b. fetch means for fetching a REPEAT instruction indicating the single instruction that is to be repeatedly executed; (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 112);

c. execute means for executing the REPEAT instruction indicating the single instruction that is to be repeatedly executed (Shridhar, column 2 line 20-column 4, line 12, Figures 1 and 2, element 116);

d. means for incrementing a program counter (Shridhar, column 2 line 20-column 4, line 12, Figures 1 and 2, element 148);

e. fetch means for fetching the single instruction (Shridhar, column 2 line 20-column 4, line 12, Figures 1 and 2, element 112); and

f. execute means for repeatedly executing the single instruction for a consecutive number of times as indicated by a count value stored in a count register (Shridhar, column 2 line 20-column 4, line 12, Figures 1 and 2, element 116, element 130) without re-fetching the single instruction and without fetching any other instruction (Shridhar, column 2 lines 20-23 and 31-45);

g. means for decrementing the count value in the register each time the single instruction is executed (Shridhar, column 2 line 20-column 4, line 12, element 150);

h. means for incrementing a program counter once the count value in the register is one of less than zero and equal to zero, thereby providing an effective data rate of one transfer every clock cycle (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 148).

2. Referring to claim 11, Shridhar has taught a processor according to claim 10, as described above, wherein said count value is stored in said count register before execution of said REPEAT instruction (Shridhar column 2 lines 20-23 and 31-45).

3. Referring to claim 12, Shridhar has taught a processor according to claim 10, as described above, wherein said REPEAT instruction includes the count value that is stored in said count register, wherein execution of the REPEAT instruction stores the count value in said count register (Shridhar, column 2 line 20-column 4, line 12).

4. Referring to claim 13, Shridhar has taught a processor according to claim 10, as described above, wherein said processor further comprises: means for incrementing the program counter

after the associated instruction has been executed for as many times as indicated by the count value (Shridhar, column 2 line 20-column 4, line 12, element 148).

5. Referring to claim 14, Shridhar has taught a processor according to claim 10, as described above, wherein processor further comprises:

a. means for decrementing said count value stored in said register each time said the instruction is executed (Shridhar, column 2 line 20-column 4, line 12, Figures 1 and 2, element 150); and

b. means for determining whether said count value is less than or equal to zero (Shridhar, column 2 line 20-column 4, line 12, Figures 1 and 2, elements 154 and 156).

2. Referring to claim 15, Shridhar has taught a processor for repeatedly executing one or more processor instructions (Shridhar, column 2 line 20-column 4, line 12, Figures 1 and 2), comprising:

a. a memory address register associated with a main memory (Shridhar, figure 1);

b. a memory control for generating memory control signals (Shridhar, figure 1);

c. a program counter for storing a memory address location of the main memory where an instruction is to be fetched (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 144);

d. an instruction register for storing an instruction that is to be executed (Shridhar, column 2 line 20-column 4, line 12, Figures 1 and 2, internal DSP registers);

e. at least one general purpose register storing a count (Shridhar, column 2 line 20-column 4, line 12, Figures 1 and 2, element 146);

f. decode and execute control logic for decoding and executing an instruction stored in the instruction register (Shridhar, column 2 line 20-column 4, line 12, Figures 1 and 2, elements 114 and 116); and

g. a state machine for controlling the fetching and repeated execution of an associated instruction (Shridhar, column 2 line 20-column 4, line 12, Figures 1 and 2, element 110);

h. the state machine configured to repeatedly execute the single instruction without refetching the single instruction (Shridhar column 2 lines 20-23 and 31-45); and

i. decrementing the count value in the register each time the single instruction is executed (Shridhar, column 2 line 20-column 4, line 12, Figures 1 and 2, element 150)

j. incrementing a program counter once the count value stored in the general purpose register is below a threshold value, thereby providing an effective data rate of one transfer every clock cycle (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 148).

2. Referring to claim 16, Shridhar has taught the processor according to claim 15, as described above, wherein said processor further comprises an instruction buffer for storing the single instruction (Shridhar, column 2 line 20-column 4, line 12, Figure 1).

3. Referring to claim 17, Shridhar has taught the processor according to claim 15, as described above, wherein said general purpose register includes a first register for storing a count value indicative of the number of times the one or more associated instructions are to be repeatedly executed (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 146).

4. Referring to claim 18, Shridhar has taught the processor according to claim 17, as described above, wherein said state machine generates signals for decrementing the count value stored in the first register (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 150).

5. Referring to claim 19, Shridhar has taught the processor according to claim 17, as described above, wherein said state machine generates a signal for executing an instruction stored in said instruction register (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 116).

6. Referring to claim 20, Shridhar has taught the processor according to claim 17, as described above, wherein said state machine generate a signal for incrementing said program counter after the associated instruction is repeatedly executed (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 148).

7. Referring to claim 21, Shridhar has taught the processor according to claim 8, as described above, wherein the means for executing the REPEAT instruction and the means for repeatedly executing the single instruction are the same means (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 110, element 116).

8. Referring to claim 22, Shridhar has taught the processor according to claim 8, as described above, wherein the means for fetching a REPEAT instruction and the means for fetching the single instruction are the same means (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 110, element 112).

9. Referring to claims 23 and 26, Shridhar has taught the processor according to claims 8 and 15, as described above, further comprising incrementing the program counter once the count

value is equal to zero (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 148).

10. Referring to claims 24 and 27, the processor according to claims 8 and 15, as described above, Shridhar has taught further comprising incrementing the program counter once the count value is less than zero (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, element 148).

11. Referring to claims 25, 28, 29 and 31, Shridhar has taught the processor according to claims 15, 8, and the method of operating a processor according to claims 2 and 3, as described above, wherein the program counter remains unchanged as the single instruction is repeatedly executed (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2, Element 144 is loaded with the same program counter value each time one instruction is repeatedly executed.).

12. Referring to claims 30 and 32, Shridhar has taught the method of operating a processor according to claims 2 and 3, as described above, wherein the program counter is effectively stalled on the single instruction until the single instruction executes the number of times indicated by the count value (Shridhar, column 2 line 20-column 4, line 12, figures 1 and 2).

Response to Arguments

13. Applicant's arguments with respect to claims filed on March 2, 2005 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L. Meonske whose telephone number is (571) 272-4170. The examiner can normally be reached on Monday-Friday, 8-4:30.

15. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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